We claim:

1. In a floating-point adder having a long path and a short path, a method of selecting the path for a subtraction operation involving two operands, each operand having a mantissa and an exponent, the method comprising:

responsive to a difference between the exponents of the two operands being greater than one, selecting the long path;

responsive to a difference between the exponents of the two operands being zero, selecting the short path;

responsive to the difference between the exponents of the two operands being one, and the mantissa of the operand with a larger exponent being in a first predetermined number range, selecting the short path; and

responsive to the difference between the exponent of the larger operand and the exponent of the smaller operand being one, and the mantissa of the larger operand being in a second predetermined number range, selecting the long path.

2. The method of claim 1, wherein the first predetermined number range consists of numbers smaller than 1.5, and the second predetermined number range consists of numbers not less than 1.5.

3. The method of claim 1, wherein the first predetermined number range consists of numbers not greater than 1.5, and the second predetermined number range consists of numbers greater than 1.5.

4. In a floating-point adder unit having two concurrent data paths, a short path and a long path, each data path producing a result for a floating-point operation involving two operands, each operand having a mantissa and an exponent, a method for selecting a result between the result produced by the short path and the result produced by the long path, comprising:

in response to the floating point operation being an addition operation, selecting the result produced by the long path;

in response to the floating point operation being a subtract operation and a difference between the exponents of the two operands being larger than 1, selecting the result produced by the long path;

in response to the floating point operation being a subtract operation and a difference between the exponents of the two operands being 0, selecting the result produced by the short path

in response to the floating point operation being a subtract operation, the difference between the exponents of the two operands being 1, and the mantissa of the operand with a larger exponent being in a first predetermined number range, selecting the result produced by the short path; and

in response to the floating point operation being a subtract operation, the difference between the exponents of the two operands being 1, and the mantissa of the operand with a larger exponent being in second predetermined number range, selecting the result produced by the long path.

5. The method of claim 4, wherein the first predetermined number range consists of numbers smaller than 1.5, and the second predetermined number range consists of numbers not less than 1.5.

6. The method of claim 4, wherein the first predetermined number range consists of numbers not greater than 1.5, and the second predetermined number range consists of numbers greater than 1.5.

7. A floating-point adder unit comprising a short path and a long path, wherein the short path does not include means for rounding a subtraction result.

8. A floating-point adder unit for performing a floating-point operation on two operands, comprising:

two concurrent data paths, a short path and a long path, each data path receiving the two operands and producing a possible result for the floating point operation involving the two operands; and

a selection logic module running concurrently with each data path and including logic circuits configured to determine whether to select the possible result from the short path or the possible result from the long path as a result of the floating-point operation, using the method as set out in any of the claims 3, 4, or 5.

9. The floating-point adder unit as in claim 7, further comprising a result selection module coupled to the short path, the long path and the selection logic module, and including logic circuits configured to select between the possible result from the

short path and the possible result from the long path a result of the floating-point operation based on the determination made by the selection logic module.

10. The floating-point adder unit of claim 8, wherein the short path does not include means for rounding a subtraction result.